

# Connie L. O'Dell

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## PROFILE

Versatile, award-winning EDA application engineer / technical marketing engineer / verification specialist, experienced in introducing formal verification, assertion-based verification, mixed-D/A simulation, and other innovative software technology into major semiconductor firms.

Innovates and responds to customer needs, to improve usability and market acceptance.

Leverages R&D effectively, and will travel as needed, to ensure customer satisfaction and sales.

## SUMMARY OF QUALIFICATIONS

**Verification:** formal verification (FV), property checking, assertion-based verification, testbench/model development, constrained random simulation, TestBuilder, hardware design spec review, synthesizable HDL, Verilog, VHDL, NCSIM, Verilog-XL, ModelSim, mixed digital/analog simulation, signal integrity, ASICs.

**Industry standards:** Volunteer and IEEE/Accellera reviewer for OVL, Sugar/PSL, and System Verilog.

**Sales engineering:** Helped many major semiconductor/electronics vendors make practical application of formal verification (technology transfer), better understand and compare product capabilities, and helped them prioritize key requests for incorporation into future versions. Helped them understand how to convert their design specs into properties to be proven/checked. Detailed technical problem diagnosis, workarounds, expediting key issues through R&D. This work was key to Cadence/BLDA FV sales.

**Technical marketing:** Marketing design verification services. Delivering technical tradeshow presentations/demos on Design Automation Conference (DAC) floor/suites for 6 years; senior technical presenter at major customer sites in western US. Learned and applied Target Account Selling (TAS).

**Technical environments and skills:** UNIX, Windows XP/2000/98, Solaris, RedHat Linux, HP-UX, PalmOS, LSF and compute farms, Globetrotter licensing/lmgrd, ksh, csh, bash, tcsh, sh, C, C++, g++, AWK, Tcl/Tk, ClearCase, Purify, competitive analysis via web/tradeshow research and Google.

**Product specification:** Wrote GUI product requirements (PRS) for Cadence's StaticCheck and complete technical requirements for point releases of FormalCheck.

**Leadership:** Small business mgmt. Mentoring, teaching, motivating teams, teamwork/communication in coordination of tasks with R&D/AEs, interviewing, advocacy and leadership in work/volunteering.

**Recent training/study/hands-on:** Verification track at BSNUG03: Synopsys Vera, OVA, System Verilog, Magellan, Assertion-based verification (ABV); Simulation case study: Self-checking testbench using Open Verilog (OVL) assertions in Silos and MTI Modelsim; System C hands-on training; FPGA design with Verilog; @HDL @Verifier; Verisity class: e, Specman, directed random test; Verilog 2001; Mentor Graphics ICX & HyperLynx GHz (simulation-based signal integrity); Perl; DVCON03, DAC03, CAV03.

**Software engineering background:** Wrote widely-used LSF farm scripts, scripts to map assertions to Sugar/PSL, to convert unsupported HDLs to supported subset & to strip out unsynthesizable constructs in Lucent Microelectronics simulation library. Ported large (100KLOC) application ATTSIM from OpenWin to XWindows, developed transmission line delay injection module, integrated ATTSIM into MGC framework, "purified" C++ applications, developed popular project management tool. Wrote/maintained corporate catalog/simulation model alignment tool. Motivated LMC and Quad design to implement Lucent needs.

**Rich CS/Math background:** Computer science/computer engineering, CAGD/CAD, graphics, 3D modeling, rendering, computational complexity, human/computer interfaces (HCI), mathematics, numerical analysis, signal processing, artificial intelligence (AI), expert systems.

## PROFESSIONAL HISTORY

CO Consulting, Inc., Boulder, CO 2003-present

**President and Principal Engineer, Design Verification Services, <http://co-consulting.net>**

- Providing contract design verification services for Colorado high-tech manufacturer, including simulation model and testbench development, simulation results analysis, hardware spec and methodology review.
- Skills: NCSIM, Signalscan, Verilog, TestBuilder, constrained random simulation, Design for Six Sigma, marketing, website design, billing, contract negotiation.

CADENCE DESIGN SYSTEMS, INC., Broomfield, CO 1998-2002

**Lead Product Engineer, FormalCheck and Assertion Verification R&D, Systems & Functional Verification Division (1999-2002)**

- Wrote AWK script to convert existing assertions to Sugar/PSL. Participated in PSL and System Verilog standardization process to ensure that common customer assertions were expressible.
- Ongoing competitive analysis of current and anticipated verification offerings includes Verplex Blacktie, Real Intent Verix, 0-In suite, Synopsys FormalVera and OVA, @HDL suite, Debussy, Verisity Specman & E.
- Helped to drive roadmap for Sugar/PSL assertion-language support to cover critical early customer needs.
- Specified new GUI and created the first system stress-tests in Clear Case, for a new verification product.
- Wrote requirements for FormalCheck 3.1-3.5 as lead FormalCheck Product Engineer, incorporating rollout requirements from 10+ of the largest US & European semiconductor/electronics companies.
- Led design/delivery of FormalCheck suite demonstrations at Design Automation Conference (DAC), 3 years.
- Led development of training materials and labs for FormalCheck and effective assertion-writing techniques. Observed AE delivery of live courses and made course improvements to make it more useful for customers.
- Applied real-world model checking techniques and FV theory to help AEs & marketing in US, Europe, Japan.
- Improved customer satisfaction with hotline/AE support by proactively tracking & documenting high-impact customer issues for Release to Manufacturing (RTM), and writing product notes for hot issues/features.
- Managed the involvement of researchers and developers in strategic customer status/partnership meetings.
- Authored and presented a seminar on clock extraction for R&D as expert on practical application and results.
- At customer request, developed new application notes that allowed customers to experiment with urgently-needed new features before fully productized, writing down clear simple procedures for users to follow. Specialized in making it simple for users to apply clock extraction, iterated reduction, various vacuity checks, auto-restrict, explicit state, and commonly-needed manual reductions.
- Worked with customers to understand need for common coverage between property checking/simulation.
- Documented customer flows (process for applying tool) and communicated to development.
- Partnered with application engineers and sales to deliver presentations to high-revenue customers both remote and face-to-face, supporting sales messages essential to that account.
- Strong spoken and written communication skills. Self-starter: worked remote from management for 12 years. Teamed up with PA/NJ development team, management to ensure product reflected customer priorities.
- Maintained technical, customer, and collateral continuity during 5 development/marketing transitions. Enthusiastically accepted as new technical contact by customer partners; rose to lead FormalCheck PE.

**Formal Verification Core Competency Engineer, Logic & Design Verification Division (1998-1999)**

- Developed and presented FormalCheck demos at Design Automation Conference, learned equivalence checking, reviewed FormalCheck specs, proposed friendly user interfaces for customer-requested features.
- Partnered with major account customers to teach FormalCheck usage, advocate their needs, support fanout.
- Consulted by Application Engineers and other Core Comps. Promoted to Product Engineering in 1999.

Lucent Technologies, Broomfield, CO

**Formal Verification Application Engineer, Bell Labs Design Automation (1995-1998)**

- Wrote application notes on clock extraction, datapath abstraction, after experimenting with new research.
- Mentored new FormalCheck AEs; wrote "Outline of FormalCheck Knowledge" defining proficiency levels.
- When FormalCheck was named "EDN Innovation of the Year", and DAC suites were over-capacity, devised and delivered large-room demos (20 people) to efficiently accommodate extra demand. Demonstrated FormalCheck 3 years at DAC.
- Wrote UNIX utilities to rewrite HDL constructs unsupported in early code, to minimize customer pain.

Lucent Technologies / AT&T, Broomfield, CO & Naperville, IL

**Min-max Digital/Analog Simulation Software Engineer / Simulation Subject Matter Expert, Bell Labs Design Automation (1985-1995)**

- Presented work at Lucent Technologies Design User Conference, as developer of major module in ATTSIM to incorporate transmission line delays into min-max simulation (both proprietary transmission-line algorithm and Quad Design's Transmission Line Calculator).
- Developed significant subsystems of ATTSIM/Mentor Graphics integration package, integration software, and Purified new C development on project to correct memory leaks.
- Specified and developed an ATTSIM/Synopsys Logic Modeling Group (LMG) simulation model integration package that incorporated min-max timing, partnering with LMG and Lucent design teams.

- Improved ATTSIM portability and usability by converting to XWindows.
- Wrote R/C delay calculation utility, in cooperation with AT&T Bell Labs research, for LAMP2 simulator.
- 10 years experience Lucent CAE/CAD software development overall; extensive remote collaboration with Bell Labs Murray Hill researchers/developers on multiple projects, to leverage the latest technology in local design flows across Lucent/AT&T.
- Studied usage and specified improved tools as Lucent system simulation Subject-Matter-Expert.
- Helped Bell Labs Design Automation evolve from a solely internal EDA provider to a visible external provider by taking on a 1-year combined support/development role, 2 years as full-time simulation Application Engineer, and a brief period in sales during the first major sales rollout.
- Demonstrated ATTSIM mixed D/A simulator in suites at Design Automation Conference for 2 years.
- Interviewed candidates, mentored summer employee, taught UNIX/Pascal classes at local schools, hosted department seminars. Briefly supported synthesis, schematic capture, ADVICE, board layout.

University of Utah, Salt Lake City, UT

Research Assistant for Alpha-1 Project / Teaching Assistant, **Computer Science Dept.** (1983-1985)

- Architected, developed, and documented 3D modeling and analysis subsystem to demonstrate thesis research in numerical & heuristic techniques for approximating noisy data with parametric B-spline curves and surfaces. Provided hooks for researchers as well as friendly end-user interfaces. Demonstrated research to DARPA sponsors. Technical session reviewer for SIGGRAPH for 2 years.
- Taught software engineering, languages (C, Pascal, Fortran, Ada), theoretical computer science, consulted, graded homework/programs, developed software package for class to use.

### TECHNICAL EXPERIENCE

- Formal verification (model checking) application specification, sales engineering, competitive analysis, technical marketing (7 years)
- Front-end applications and algorithm development for EDA Software (10 years)
- Extensive teaching and mentoring experience, interviewing, delegation of tasks, leadership
- C and UNIX Programming (10 years)
- Original research (2 years); Productizing research for practical application (7 years)
- Solaris, RedHat Linux, HP-UX, PalmOS, XWindows, UNIX, Windows XP, 98 & 2000, Platform LSF, Microsoft Outlook, Word, PowerPoint, Publisher. Website development and maintenance.
- GUI / UI specification, coordination with vendors on standards, prototyping, integration
- Languages: Strong in Sugar/PSL, OVL, Verilog, VHDL, C, AWK, shell programming/portability
- Also: Tcl/Tk, C++, LISP, HTML, Clear Case, Purify, survival Spanish & French, cross-functional teams, stage-gate quality process, object-oriented, numerical analysis, signal processing, expert systems (AI)
- Mentor for Dean Kamen's FIRST Robotics Program / presenter for prospective Denver schools, 2003.
- Training: Managing Personal Growth, Effective Teams, HTML, C++, Perl, Target Account Selling, Visual C++, Java, Microsoft Project, Verisity Specman, 'e', and random stimulus generation.

### AWARDS

**2000 Cadence Bravo Award**, *Demonstrated self-motivated commitment to actively improve product quality of FC3.1 by flexibly applying my own varied technical skills & enlisting team efforts*

**1997 EDN Innovation of the Year Award, Best New Product**, *Member of winning team*

### PUBLICATIONS

**Cohen, E. and O'Dell, C. L., "A Data Dependent Parametrization for Spline Approximation,"**

Mathematical Methods in Computer Aided Geometric Design (Lyche/Schumaker), Academic Press, 1989.

**O'Dell, C. L. F., "Approximating Data with Parametric B-splines,"** Master's thesis, Department of Computer Science, University of Utah, December 1985.

My Portfolio – EDA Industry reports, OVL case study, Application notes: <http://co-consulting.net>

Report on new formal verification products at DAC03 from 0-In, Jasper Design Automation's JasperGold, Synopsys Magellan, @HDL and IBM, for John Cooley's ESNUG. To be published.

### EDUCATION

**M.S., Computer Science (Computer Graphics, CAGD)**

University of Utah, Salt Lake City, Utah, 1985

**B.S., Mathematics, Cum Laude**

University of Utah, Salt Lake City, Utah, 1982